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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/974,721	10/09/2001	Jian Zhou	M-11928 US	7841

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EXAMINER	
LAROSE, COLIN M	

ART UNIT	PAPER NUMBER
2624	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/974,721	ZHOU ET AL.	
	Examiner	Art Unit	
	Colin M. LaRose	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16,22 and 24-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-16,22 and 25* is/are allowed.

6)☒ Claim(s) *1-3,8 and 24* is/are rejected.

7)☒ Claim(s) *4-7 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Arguments and Amendments

1. Applicant's arguments and/or amendments dated 20 January 2007, have been entered and made of record.

Response to Amendments and Arguments

2. Regarding claim 1, Applicant asserts that Scheiner does not learn an alignment feature at multiple layers on a golden wafer, as required by the claim (see Remarks, p. 6). According to Applicant, there is no teaching or disclosure in Scheiner that would lead one to believe that underlying alignment features contained in intermediate layers are learned and stored (Remarks, p. 6).

Applicant "is not aware of any disclosure that Scheiner is related to measuring a characteristic of a patterned article at various manufacturing states of the wafer, i.e., at different wafer layers" (Remarks, p. 6). However, as best understood by the Examiner, Scheiner's method is relevant to the measurement of any layer of a wafer during or after the manufacturing process. For example, Scheiner recognizes that patterns are formed on wafers in multiple-layer stacks, and during various manufacturing steps, there is a need to measure the thickness or other characteristics of an uppermost or other layer of a semiconductor (column 1/14-19). In addition, since the manufacturing steps are carried out layer-by-layer, "thickness measurements are performed separately after each manufacturing step" (column 2/63-66). Accordingly, Scheiner's measurements can occur for any layer in the manufacturing process.

When Scheiner performs a measurement for a site of interest contained in a given layer, an alignment feature is extracted, or "learned," and stored in the recipe design file (column 6/66 et seq.). The alignment feature is used for aligning, or "de-skewing," the wafer prior to or after the measurements of the site of interest (column 8/1-2).

Therefore, for a given site on the wafer corresponding to a first layer of the manufacturing process, Scheiner learns an alignment pattern to be used for de-skewing the wafer. Subsequently, that alignment pattern and its coordinates are saved in a recipe later used for de-skewing similar wafers to be measured.

Scheiner's method is applicable to any layer of the manufacturing process. Thus, if a subsequent layer is formed over the "first layer" and measurements are to be performed at the same site corresponding to the subsequent layer, then the wafer is aligned in order to locate the measurement site (column 7/66-67—"To locate [a] measurement site, a wafer alignment procedure is typically performed"). That is, an alignment pattern is learned and stored in the recipe in order to de-skew wafers when measurements are performed at the same site and in the same layer.

The learning and storage of Scheiner's alignment patterns at various layers corresponding to a given site or location on a golden wafer does not appear to be expressly set forth in Scheiner's disclosure. However, such is considered to be implicitly disclosed insofar as Scheiner's measurements can be performed on any given layer of a wafer, and aligning the wafer is necessary when performing measurements. "[I]n considering the disclosure of a reference, it is proper to take into account not only specific teachings of the reference but also the inferences

which one skilled in the art would reasonably be expected to draw therefrom." In re Preda, 401 F.2d 825, 826, 159 USPQ 342, 344 (CCPA 1968); MPEP § 2144.01.

Accordingly, Applicant's arguments are not considered persuasive, and the previous rejection of claim 1 has been maintained.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 8, and 24 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,556,947 by Scheiner et al. ("Scheiner").

Scheiner discloses a system for measuring patterns formed on wafers using a "recipe." The recipe contains "alignment features," which are unique patterns found in each die on the wafer and are used for performing wafer alignment of wafers that are "similar." See column 1/20-35 and 8/1-11. In addition to containing the alignment feature, the recipe contains "all necessary information" regarding a specific site on a wafer. Column 7/17-20.

The alignment features, as well as the other reference data, are extracted from a "golden" wafer that contains all of the representative structures on the wafer at each layer of the wafer. Column 2/54-62. These extracted alignment features are then used to align the wafer when

measurements are performed on the golden wafer at a given site. Column 2/63 through column 3/5 and column 7/66 et seq.

Therefore, regarding claim 1, Scheiner discloses a method for forming a recipe for de-skewing wafers, comprising:

learning a first pattern at a de-skew site on a first wafer layer (column 8/2-5: Scheiner extracts an alignment pattern at a given site on a first layer of the golden wafer);

saving the first pattern and its location in a recipe for de-skewing wafers (column 8/2-5: Scheiner records the extracted alignment pattern, including information pertaining to its location, in a recipe that is used for "aligning," or de-skewing, wafers);

learning a second pattern at the de-skew site on a second wafer layer (columns 2/63—3/5 and 8/2-5: for a subsequent layer in the manufacturing process, Scheiner extracts an alignment pattern at the given site on the golden wafer); and

saving the second pattern in the same recipe for de-skewing wafers (column 8/2-5: Scheiner records the second extracted alignment pattern, including information pertaining to its location, in the recipe that is used for "aligning," or de-skewing, wafers when performing measurements at the site in the same layer).

Regarding claim 8, Scheiner discloses saving a file name of a file including the first pattern (column 1/65-67).

Regarding claim 24, Scheiner teaches that the first wafer layer is a top surface of said wafer and said second wafer layer is the top surface of said wafer after said wafer is processed

(i.e. Scheiner extracts the reference information for the golden wafer after each processed layer – see column 2/63-67).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,556,947 by Scheiner et al. ("Scheiner") in view of U.S. Patent 6,240,208 by Garakani et al. ("Garakani").

Regarding claim 2, Scheiner does not disclose learning the first pattern comprises determining a score of uniqueness for the first pattern.

Garakani discloses a method for identifying reference patterns to be utilized for aligning wafers. In particular, Garakani discloses that it is advantageous to select reference patterns that

are unique. Garakani teaches determining the uniqueness of potential reference patterns, and selecting from among the reference patterns on the basis of their uniqueness scores. For example, in figure 2, the uniqueness of various reference patterns is measured at step 240, and the suggested reference patterns are ordered at step 260 based in part on the uniqueness scores.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Scheiner by Garakani to determine a score of uniqueness for the first pattern to be learned, since Garakani discloses that it is advantageous to select a reference pattern utilized for aligning semiconductor wafer layers that is unique, and determining a score of uniqueness indicates whether a pattern to be learned is unique (see e.g. column 1, lines 19-32; column 6, lines 58-67).

Regarding claim 3, Garakani discloses selecting a first pattern that has a parameter value (e.g. uniqueness) greater than a threshold (see column 7, lines 51-59). Therefore, that pattern that is learned and saved according to Scheiner's teachings is sufficiently unique.

Allowable Subject Matter

8. Claims 9-16, 22, and 25, as previously indicated, are allowable.

9. Claims 4-7 and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Colin M. LaRose whose telephone number is (571) 272-7423. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bhavesh Mehta, can be reached on (571) 272-7453. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would

like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000. Any inquiry of a general nature or relating to the status of this application or proceeding can also be directed to the TC 2600 Customer Service Office whose telephone number is (571) 272-2600.

Colin M. LaRose
Group Art Unit 2624
19 July 2007

BHAVESH M MEHTA
SUPERVISORY PATENT EXAMINER
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